XT1D110 Datasheet

Ver-1.0

General Description

The XT1D110 is a 10 output differential high performance clock buffer.

The input can be selected from two differential inputs or one crystal input. The selected input clock is distributed to two banks of 5 differential outputs and one LVCMOS output. Both differential output banks can be independently configured as LVPECL, LVDS or HCSL mode, or disabled. The LVCMOS output has a synchronous enable input for glitch-free operation when enabled or disabled.

The device is designed for a signal fan out of high-frequency, low phase-noise clock. It is designed to operate from a 3.3V/2.5V core power supply, and 3 independent output supplies: 3.3V/2.5V.

Applications

- Clock distribution and level translation for ADCs, DACs, Multi-gigabit ethernet, XAUI, SATA/SAS, SONET/SDH, CPRI, high frequency back planes
- Switches, routers, line Cards, timing cards
- Servers, computing, PCI express (PCIe 3.0, 4.0)
- Remote radio units and base band units
- Test and Measurement

Features

- Two differential reference clock pairs
- Input pairs can accept the following differential input levels:

  LVPECL, LVDS, HCSL, HSTL or single ended
- Crystal Input accepts 10MHz to 100MHz Crystal or Single Ended Clock.

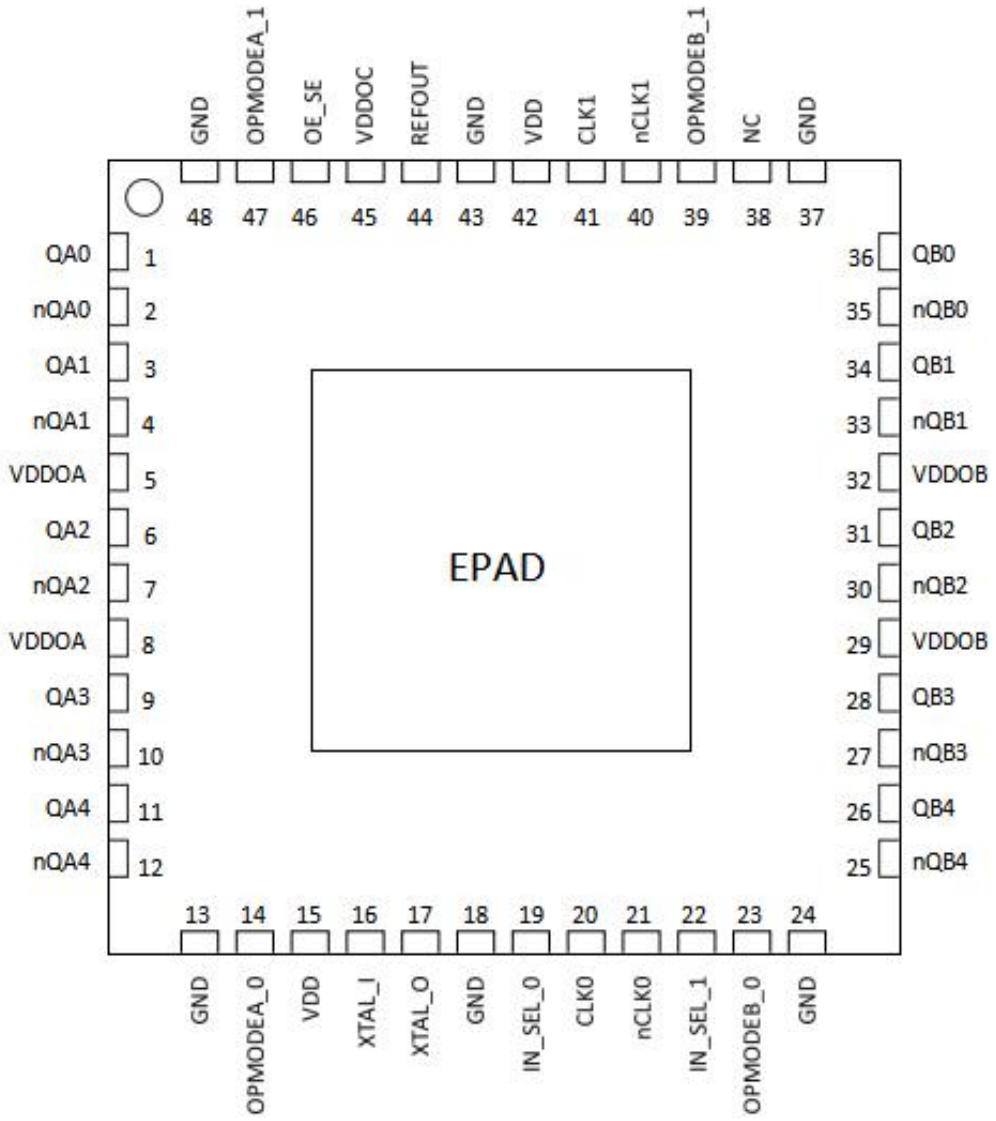
  Maximum output frequency

LVPECL	- 2GHz
LVDS	- 2GHz
HCSL	- 350MHz
LVCMOS	- 250MHz
- Two banks, each has five differential output pairs that can be separately configured as LVPECL or LVDS or HCSL or Hi-Z
- One single-ended reference output with synchronous enable to avoid glitch
- Output skew: 30ps (typical)
- Part-to-part skew: 60ps (typical)

  Additive RMS phase jitter @ 156.25MHz:
  50 fs RMS (10kHz - 20MHz), @ 3.3V/ 3.3V
- Supply voltage modes:

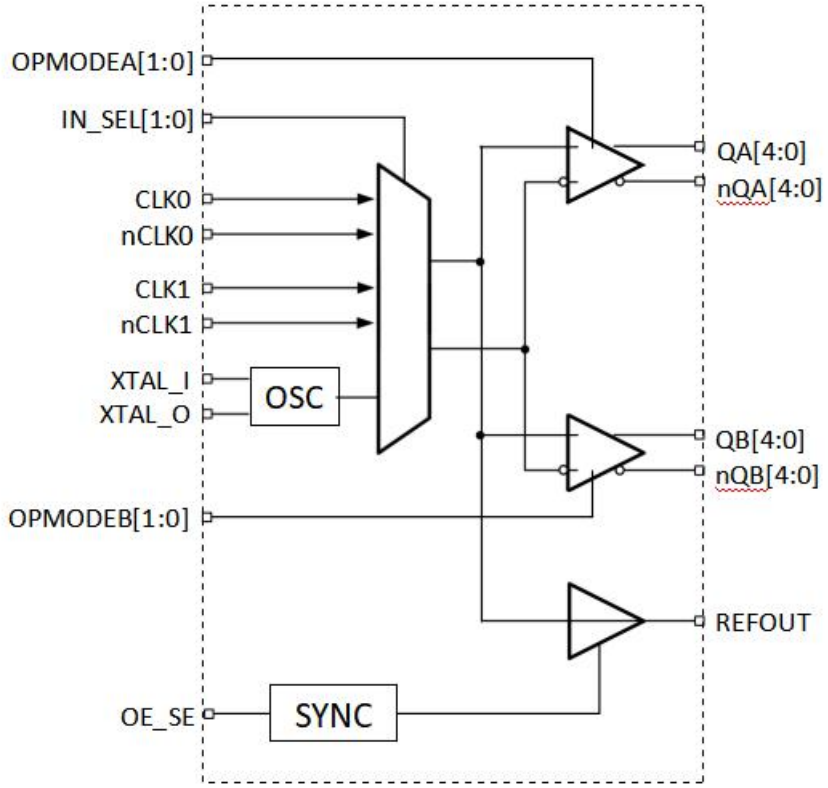
VDD	VDDO
3.3V	3.3V
3.3V	2.5V
2.5V	2.5V
- Operation temperature range: -40°C to 85°C:
- Package: 48-pin, 7mm*7mm QFN

Pin Configuration：



48-pin QFN (Top View)

Block Diagram：



Pin Descriptions：

Number	Name	Type	Description
1	QA0	Output	Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
2	nQA0	Output	Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
3	QA1	Output	Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
4	nQA1	Output	Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
5	VDDOA	Power	Power supply pins for Bank A outputs. 3.3V or 2.5V.
6	QA2	Output	Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
7	nQA2	Output	Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
8	VDDOA	Power	Power supply pins for Bank A outputs. 3.3V or 2.5V.
9	QA3	Output	Bank A differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
10	nQA3	Output	Bank A differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
11	QA4	Output	Bank A differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
12	nQA4	Output	Bank A differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
13	GND	Ground	Ground.
14	OPMODEA_0	Input/Pulldown	Output mode select for Bank A. See Table 2 for functions, LVCMOS/LVTTL interface levels.
15	VDD	Power	Power supply pin for Crystal core and input blocks, 3.3V or 2.5V.
16	XTAL_I	Input	Crystal oscillator input pin.

17	XTAL_O	Output	Crystal oscillator output pin.
18	GND	Ground	Ground.
19	IN_SEL_0	Input/Pulldown	Input clock selection. See Table 1 for functions, LVCMOS/LVTTL interface levels.
20	CLK0	Input/Pulldown	Reference input 0. Internally biased to ground.
21	nCLK0	Input/Pullup-Pulldown	Inverting reference input 0. Internally biased to 0.5*VDD.
22	IN_SEL_1	Input/Pulldown	Input clock selection. See Table 1 for functions, LVCMOS/LVTTL interface levels.
23	OPMODEB_0	Input/Pulldown	Output mode select for Bank B. See Table 2 for functions, LVCMOS/LVTTL interface levels.
24	GND	Ground	Ground.
25	nQB4	Output	Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
26	QB4	Output	Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
27	nQB3	Output	Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
28	QB3	Output	Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
29	VDDOB	Power	Power supply pins for Bank B outputs. 3.3V or 2.5V.
30	nQB2	Output	Bank B differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
31	QB2	Output	Bank B differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
32	VDDOB	Power	Power supply pins for Bank B outputs. 3.3V or 2.5V.
33	nQB1	Output	Bank B differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
34	QB1	Output	Bank B differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
35	nQB0	Output	Bank B differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
36	QB0	Output	Bank B differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
37	GND	Ground	Ground.
38	NC	Unused	No connect pin.
39	OPMODEB_1	Input/Pulldown	Output mode select for Bank B. See Table 2 for functions, LVCMOS/LVTTL interface levels.
40	nCLK1	Input/Pull-Pulldown	Inverting reference input 1. Internally biased to 0.5*VDD.
41	CLK1	Input/Pulldown	Reference input 1. Internally biased to ground.
42	VDD	Power	Power supply pin for Crystal core and input blocks, 3.3V or 2.5V.
43	GND	Power	Ground.
44	REFOUT	Output	Single-ended reference clock output. LVCMOS interface levels.
45	VDDOC	Power	Power supply pin for REFOUT output.
46	OE_SE	Input/Pulldown	Synchronous output enable for REFOUT. See Table 3 for functions, LVCMOS/LVTTL interface levels.
47	OPMODEA_1	Input/Pulldown	Output mode select for Bank A. See Table 2 for functions, LVCMOS/LVTTL interface levels.
48	GND	Power	Ground.